UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,470	09/05/2003	Arvind Halliyal	G0533	8691

7590 03/24/2004

Thomas W. Adams
Renner, Otto, Boisselle & Sklar, LLP
Nineteenth Floor
1621 Euclid Avenue
Cleveland, OH 44115-2191

EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,470	HALLIYAL ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-20* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/05/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on September 05, 2003.

The references cited on the PTO -1449 form have been considered except the "OTHER ART" (the related documents have not been provided).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1 – 7** and **9 – 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (US Patent No. 6,407,435 IDS).

Regarding claim **1**, Ma et al. disclose a semiconductor device having a composite dielectric layer, comprising: a semiconductor substrate (fig. 3 112), alternating sub-layers (fig. 3, 116) comprising a first dielectric material (fig. 3, 130) and a second dielectric material (fig. 3, 140) on the semiconductor substrate, the sub-layers forming a composite dielectric layer having at least two sub-layers of at least one of the first dielectric material and the second dielectric material, wherein one of the first dielectric material and the second dielectric material is a high-K dielectric material and

an other of the first dielectric material and the second dielectric material is a standard-K dielectric material comprising aluminum oxide (col. 4, lines 24+);

Ma et al. do not explicitly teach a reaction product of the high-K dielectric material and the standard-K dielectric material. However, Ma et al. teach a step (550) which is the annealing of the multilayer dielectric stack (col. 7, lines 19 – 28) similar to that of applicant's specification (in page 15, lines 6 – 10) stating that "*The composite dielectric layer, comprising the reaction product of the high-K dielectric material and the standard-K dielectric material, is formed by annealing the layered dielectric structure at an elevated temperature. The reaction product includes the elements of both the high-K dielectric material and the standard-K dielectric material*". It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the a reaction product of the high-K dielectric material and the standard-K dielectric material in order to reduce surface roughness, crystallinity and electrical leakage which is used in gate dielectric.

Regarding claim **2**, Ma et al. disclose the standard-K dielectric material further comprises at least one of silicon dioxide, silicon nitride and aluminum oxide (col. 4, lines 32 – 36).

Regarding claim **3**, Ma et al. disclose the high-K dielectric material comprises at least one of hafnium oxide, zirconium oxide, tantalum oxide (col. 4, lines 36 – 46).

Regarding claim **4**, Ma et al. disclose the claimed invention of claim 1 but do not explicitly teach the reaction product comprises a high-K derived metal atom, an aluminum atom and an oxygen atom. However, it is known and also stated in the

application specification that "*the high-K dielectric material is hafnium oxide and the standard-K dielectric material is aluminum oxide, the reaction product is an aluminate compound containing hafnium, aluminum and oxygen*" (page 15, lines 19 – 21). The multilayer dielectric stack in Ma et al. comprising hafnium oxide and aluminum oxide is annealed at an elevated temperature similar to that of the applicant's process. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the reaction product comprises a high-K derived metal atom, an aluminum atom and an oxygen atom in order to reduce surface roughness, crystallinity and electrical leakage which is used in gate dielectric.

Regarding claims **5** and **6**, Ma et al. disclose the first and second dielectric material can be either high-K or standard-K dielectric material in a reverse order (col.4, lines 53 – 56).

Regarding claim **7**, Ma et al. disclose that the multilayer dielectric stack is: $Al_2O_3/ZrO_2/ Al_2O_3/ ZrO_2/ Al_2O_3/ ZrO_2$. As discussed in claims 1 and 4 above, after annealing in an elevated temperature a reaction product layer appears between high-K material and standard-K material. Therefore, the composite dielectric layer in Ma et al. comprising: sub-layers (Al_2O_3/ZrO_2), a reaction production layer (not shown) and a sub-layers (Al_2O_3/ZrO_2).

Regarding claim **9**, Ma et al. disclose the number or patterns of composite dielectric layers could repeat many times (fig. 3; col. 4, lines 47 – 48).

Regarding claim **10**, Ma et al. disclose that the multilayer dielectric stack is: $Al_2O_3/ZrO_2/ Al_2O_3/ ZrO_2/ Al_2O_3/ ZrO_2$..... As discussed in claims 1 and 4 above, after

annealing in an elevated temperature a reaction product layer appears between high-K material and standard-K material. Therefore, the composite dielectric layer in Ma et al. comprising: pair of sub-layers ($Al_2O_3/ZrO_2/Al_2O_3/ZrO_2$), a reaction production layer (not shown) and a pair of sub-layers ($Al_2O_3/ZrO_2/ Al_2O_3/ZrO_2$).

Regarding claim **11**, Ma et al. disclose the composite dielectric layer (fig. 1, 16/ fig. 3, 116) is a gate dielectric layer in the semiconductor device (col. 3, lines 36 – 46; col. 4, lines 26 – 31).

Regarding claim **12**, Ma et al. disclose the composite dielectric layer (fig. 1, 16/ fig. 3, 116) is a gate dielectric layer formed on the semiconductor substrate (Fig. 1, 12; fig. 3, 112; col. 3, lines 36 – 46; col. 4, lines 26 – 31).

Regarding claim **13**, Ma et al. disclose a semiconductor device having a composite dielectric layer, comprising: a semiconductor substrate (fig. 3 112); a composite gate dielectric layer (fig. 3, 116); the composite gate dielectric comprising a first and a second dielectric material, wherein one of the first dielectric material and the second dielectric is a high-K material an other of the first dielectric material and the second dielectric material is a standard-K dielectric material (Al_2O_3) (col. 4, lines 24+);

Ma et al. do not explicitly teach a reaction product of the high-K dielectric material and the standard-K dielectric material; and the reaction product comprises a high-K derived metal atom, an aluminum atom and an oxygen atom. However, Ma et al. teach a step (550) which is the annealing of the multilayer dielectric stack (col. 7, lines 19 – 28) similar to that of applicant's specification (in page 15, lines 6 – 10) stating that "*The composite dielectric layer, comprising the reaction product of the high-K dielectric*

material and the standard-K dielectric material, is formed by annealing the layered dielectric structure at an elevated temperature. The reaction product includes the elements of both the high-K dielectric material and the standard-K dielectric material" and "*the high-K dielectric material is hafnium oxide and the standard-K dielectric material is aluminum oxide, the reaction product is an aluminate compound containing hafnium, aluminum and oxygen"* (page 15, lines 19 – 21). It is noted that he multilayer dielectric stack in Ma et al. comprising hafnium oxide and aluminum oxide is annealed at an elevated temperature similar to that of the applicant's process. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the a reaction product of the high-K dielectric material and the standard-K dielectric material; and the reaction product comprises a high-K derived metal atom, an aluminum atom and an oxygen atom in order to reduce surface roughness, crystallinity and electrical leakage which is used in gate dielectric.

Regarding claim **14**, Ma et al. disclose the standard-K dielectric material further comprises at least one of silicon dioxide, silicon nitride and aluminum oxide (col. 4, lines 32 – 36).

Regarding claim **15**, Ma et al. disclose the high-K dielectric material comprises at least one of hafnium oxide, zirconium oxide, tantalum oxide (col. 4, lines 36 – 46).

Regarding claim **16**, Ma et al. disclose a semiconductor device having a composite dielectric layer, comprising: a semiconductor substrate (fig. 3, 112); alternating sub-layers (fig. 3, 116) comprising a first dielectric material (fig. 3, 130) and a second dielectric material (fig. 3, 140) on the semiconductor substrate, the sub-layers

forming a composite dielectric layer having from 3 to about 10 sub-layers of the first dielectric material and the second dielectric material (col. 4, lines 46 – 48), each pair of sub-layers separated by a sub-layer of a reaction product of the high-K dielectric material and the standard-K dielectric material, wherein one of the first dielectric material and the second dielectric material is a high-K dielectric material and an other of the first dielectric material and the second dielectric material is a standard-K dielectric material comprising aluminum oxide (Al_2O_3) (col. 4, lines 24+).

Ma et al. do not explicitly teach a reaction product of the high-K dielectric material and the standard-K dielectric material. However, Ma et al. teach a step (550) which is the annealing of the multilayer dielectric stack (col. 7, lines 19 – 28) similar to that of applicant's specification (in page 15, lines 6 – 10) stating that "*The composite dielectric layer, comprising the reaction product of the high-K dielectric material and the standard-K dielectric material, is formed by annealing the layered dielectric structure at an elevated temperature. The reaction product includes the elements of both the high-K dielectric material and the standard-K dielectric material*". It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the a reaction product of the high-K dielectric material and the standard-K dielectric material in order to reduce surface roughness, crystallinity and electrical leakage which is used in gate dielectric.

Regarding claim **17**, Ma et al. disclose the standard-K dielectric material further comprises at least one of silicon dioxide, silicon nitride and aluminum oxide (col. 4, lines 32 – 36).

Regarding claim **18**, Ma et al. disclose the high-K dielectric material comprises at least one of hafnium oxide, zirconium oxide, tantalum oxide (col. 4, lines 36 – 46).

Regarding claim **19**, Ma et al. disclose the composite dielectric layer (fig. 1, 16/ fig. 3, 116) is a gate dielectric layer in the semiconductor device (col. 3, lines 36 – 46; col: 4, lines 26 – 31).

Regarding claim **20**, Ma et al. disclose the composite dielectric layer (fig. 1, 16/ fig. 3, 116) is a gate dielectric layer formed on the semiconductor substrate (Fig. 1, 12; fig. 3, 112; col. 3, lines 36 – 46; col. 4, lines 26 – 31).

Allowable Subject Matter

4. Claim **8** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is an examiner's statement of reasons for the indication of allowable subject matter: Claims **8** is allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

a substantially uniform layer (fig. 1, 110rp) of the reaction production of the first dielectric material and the second dielectric material.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran

March 17, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800